AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 20, and continuing to page 1, line 23, as follows:

It is often desired, and indeed sometimes required, that the delay can be varied by a control signal. Commonly, there is a desire for the delay to be a certain fraction of a period, or an integer multiple of such a fraction. In such cases, a Delay-Locked-Loop (DLL) is often used. Usually, a DLL is designed by means of active circuits, most commonly inverters. However, in such DLL[[:]]s, a fixed number, N, of delay cells is used, which means that only phase delays of M/N*360°, where 0<M<N, can be obtained.

Please amend the caption at page 1, line 28, as follows:

BRIEF SUMMARY ~~OF THE INVENTION~~

Please amend the paragraph beginning at page 2, line 1, and continuing to page 2, line 4, as follows:

This need is addressed by ~~the present invention in that it discloses~~ a delay-locked loop circuit with input means for a signal that is to be delayed, the input means comprising means for splitting said input signal into a first and a second branch.

Please amend the paragraphs beginning at page 2, line 25, and continuing to page 2, line 27, as follows:

Fig 2 schematically shows the principle behind a delay-locked loop according to ~~the invention~~an example embodiment, and

Fig 3 shows a more detailed drawing of a delay component of ~~the invention~~an example embodiment.